1-23. (Cancelled).

24. (Previously Presented) A double gate transistor comprising:

a channel region;

a top gate above said channel region;

a bottom gate below said channel region; and

spacers adjacent said top gate and said bottom gate, wherein said spacers comprise a material that is independent of the material of said top gate and said bottom gate.

25. (Previously Presented) The transistor in claim 24, wherein said top gate and said bottom gate comprise the same material.

26. (Previously Presented) The transistor in claim 24, wherein said spacers have structural indicia indicating that said spacers comprise a deposited insulator.

27. (Previously Presented) The transistor in claim 24, further comprising source and drain regions adjacent said top gate and said bottom gate, wherein said spacers separate said source and drain regions from said top gate and said bottom gate.

28. (Previously Presented) the transistor in claim 24, wherein said spacers comprise upper spacers and lower spacers separated by said channel region.

29. (Previously Presented) A double gate transistor comprising:

a channel region;

a top gate above said channel region;

a bottom gate below said channel region; and

spacers in direct contact with said top gate, wherein said spacers comprise lower spacers in direct contact with a lower section of said top gate and upper spacers in direct contact with an upper section of said top gate, wherein said lower spacers are different than said upper spacers.

30. (Previously Presented) A double gate transistor comprising:

a channel region;

a top gate above said channel region;

a bottom gate below said channel region; and

spacers in direct contact with said top gate,

wherein said spacers comprise lower spacers in direct contact with a lower section of said top gate and upper spacers in direct contact with an upper section of said top gate, and

wherein said lower spacers comprises a different material than said upper spacers.

31. (Previously Presented) The transistor in claim 29, further comprising source and drain regions adjacent said top gate, wherein said lower spacers are adjacent said source and drain regions and said upper spacers are at a level above said source and drain regions.

32. (Previously Presented) The transistor in claim 29, wherein said upper spacers are above said channel region.

33. (Previously Presented) The transistor in claim 29, further comprising third spacers adjacent said bottom gate.

34. (Previously Presented) The transistor in claim 29, further comprising source and drain regions adjacent said lower section of said top gate.

35. (Previously Presented) A double gate transistor comprising:

a channel region;

a top gate above said channel region;

a bottom gate below said channel region;

spacers in direct contact with said top gate, wherein said spacers comprise lower spacers in direct contact with a lower section of said top gate and upper spacers in direct contact with an upper section of said top gate, and wherein said lower spacers are different than said upper spacers;

source and drain regions adjacent said top gate, wherein said lower spacers are adjacent said source and drain regions; and

silicide regions along upper portions of said source and drain regions, wherein said

silicide regions are adjacent a point where said upper spacers meet said lower spacers.

36. (Previously Presented) A double gate transistor comprising:

a channel region;

a top gate above said channel region;

a bottom gate below said channel region;

spacers in direct contact with said top gate, wherein said spacers comprise lower spacers in direct contact with a lower section of said top gate and upper spacers in direct contact with an upper section of said top gate;

source and drain regions adjacent said top gate, wherein said lower spacers are adjacent said source and drain regions; and

silicide regions along upper portions of said source and drain regions,

wherein said silicide regions are adjacent a point where said upper spacers meet said lower spacers, and

wherein said lower spacers comprises a different material than said upper spacers.

37. (Previously Presented) The transistor in claim 35, wherein said upper spacers and said lower spacers are above said channel region.

38. (Previously Presented) The transistor in claim 35, further comprising third spacers adjacent said bottom gate.